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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,122	03/27/2001	Timothy Jerry Schimke	ROC920000254US1	9560

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BRACEWELL & PATTERSON, LLP
INTELLICTUAL PROPERTY LAW
P.O. BOX 969
AUSTIN, TX 78767-0969

EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 08/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,122	SCHIMKE ET AL.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20010625*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The present Office action is in response to application dated 27 March 2001.

Claims 1-34 are pending in the application. All claims have been examined.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 25 June 2001 was filed after the mailing date of the application on 27 March 2001. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to because

- Figure 1, black boxes "120", "130", "140", "150" should be labeled as to their function.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- Figure 2, "235", "255"

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The abstract of the disclosure is objected to because

- Line 21, "is" should read "are".

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori [US 6,678,839 B2] in view of Odenwald [US 6,671,727 B1].

Regarding claim 1, Mori teaches a method (see Title) for accurately determining a device location (see column 2, lines 10-11) in an arbitrated loop (see column 1, line 15) having devices, where each of the devices has a port bypass circuit (see Abstract; "plural devices 200" and "port bypass circuit 210"). The port bypass circuits are enabled and the arbitrated loop is initialized (see column 3, line 64). An *initial* logical address is set (see column 3, line 56). The cited art cites disabling a port bypass circuit associated with a selected device and identifying a physical location (see column 2, lines 1-7). The initial logical address is stored and the port bypass circuit associated with the selected device is enabled (see column 3, lines 50-60). The process is repeated for the devices (see column 4, lines 14-15; Abstract; column 9, lines 56-57).

Nonetheless, the cited reference does not teach a "unique identifier" and "physical slot location" being "mapped", as claimed. Regarding this limitation, Odenwald explicitly teaches a permanent "unique identifier" (see column 1, lines 39-47). Furthermore, the Odenwald reference discloses "mapping" (see column 2, line 14) for "unique identifiers" and "physical address identifiers". Accordingly, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to maintain constant device identification regardless of what happens in the loop, in terms of physical location of the devices (see Odenwald, column 2, lines 8-28). This is presented by the Odenwald references as "persistent target identification".

As for claim 2, Mori teaches determining a set of valid addresses for the devices (see column 3, line 59).

As for claim 3, Mori teaches an *initial address* (see column 3, line 56) that does not correspond to the set of valid physical addresses (for the rest of the devices). Nonetheless, it does not teach an *initiator*. Regarding this limitation, Odenwald teaches an initiator (see column 2, line 23; Figure 1, "100"). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to implement a method that would maintain target identification in a Fibre Channel environment (see Odenwald).

As per claim 4, Mori teaches disabling a port bypass circuit associated with a selected device (see "bypass") and determining a logical address for the device (see column 3, line 59-61; Figure 1, "200").

As for claims 5 and 6, Mori does not teach the step of comparing the logical addresses with the physical slot location of the selected device. Furthermore, the reference fails to teach reporting a *fault condition* in response to these not being identical. Regarding this limitation, Odenwald teaches a method for maintaining constant mapping (see column 2, line 14) in order to avoid a fault condition. Moreover, Odenwald mentions the condition where the logical address and physical locations are not identical (see column 2, lines 2-13). Accordingly, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to maintain constant device identification regardless of what happens in the loop, in terms of physical location of the devices.

As for claim 7, Mori teaches disabling a port bypass circuit associated with a selected device (see "bypass") and determining a logical address for the device (see column 3, line 59-61; Figure 1, "200").

As per claim 8, Mori explicitly teaches an arbitrated loop as Fibre channel arbitrated loop (FC-AL) (see column 1, line 15).

As per claim 9, Mori does not teach a "unique identifier" as a "world wide unique address, WWID", as claimed. Nonetheless, Odenwald explicitly teaches a world wide unique identifier, according to the FC (Fibre channel) standard (see column 1, lines 39-46). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the disclosures

in order to implement a reliable method for target device identification (as presented by Odenwald).

As per claim 10, Mori does not teach a "unique identifier" and "physical slot location" as saved "utilizing a first table", as claimed. Regarding this limitation, Odenwald teaches a table where physical location as well as unique identifiers are saved (see Figure 4(a)).

As for claim 11, Mori cites disabling a port bypass circuit associated with a selected device and identifying a physical location (see column 2, lines 1-7). However, Mori does not teach storing unique identifiers in a second table. Regarding this aspect of the claim, Odenwald teaches storing "unique identifiers" in a table (see Figure 4(b)), as well as "other methods of forming the associations" (see column 5, lines 1-15). At the time the invention was made, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to maintain constant device identification regardless of what happens in the loop, in terms of physical location of the devices (see Odenwald, column 2, lines 8-28).

As for claim 12, Mori does not teach *mapping* "unique identifiers" to obtain a "physical slot location". However, Odenwald explicitly teaches, "mapping" in order to provide persistent target identification (see column 2, lines 47-53). This mapping allows the method to obtain a physical slot location (see column 2, lines 32-36).

Regarding claim 13, this is oriented to the *computer program product* for implementing the steps (a)-(f) as presented in method claim 1. The combination of references presented in the present

Office action teaches or suggests all the limitations corresponding to the method. Therefore, the combination of disclosures also teaches or suggests the limitations corresponding to the computer product for implementing the method. Claims 14-23 contain limitations for the computer program product, which correspond to method claims 2-12. These claims are rejected under the same rationale.

Regarding claim 24, this is oriented to the *arbitrated loop network* implementing the steps (a)-(f) as presented in method claim 1. The combination of references presented in the present Office action teaches or suggests all the limitations corresponding to the method. Therefore, the combination of disclosures also teaches or suggests the limitations corresponding to the loop network system implementing the method. Dependent claims 25-34 contain limitations for the arbitrated loop system, which correspond to method claims 2-12. These claims are rejected under the same rationale.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Oldfield et al. [US 20020012342 A1] fibre channel arbitrated loop dynamic loop sizing.
- Wilson [US 6,151,331 A] teaches method and system for discovering the location of a storage device.
- Wilson [US 6,199,112 B1] teaches system and method for resolving fibre channel device addresses on a network using the device's fully qualified domain name.

- JP 2001007831 A discloses failure location and recovery in FC-AL systems.
- Mc Carty [EP 0858200 A2] teaches system and method for controlling multiple initiators in a fibre channel environment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 9:30-6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

alc
30 August 2004

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100